IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A semiconductor device comprising:

a semiconductor layer including an element formation region;

an isolation surrounding the sides of the element formation region;

source/drain regions provided in the element formation region of the semiconductor layer;

a gate dielectric provided on the element formation region;

a gate electrode extending from the top of the gate dielectric to above the top of the isolation; and

a sidewall made of a dielectric, provided continuously along sides of the gate electrode and discontinued at part of the sides of the gate electrode excluding part thereof located on the element formation region,

wherein the sidewall is formed by subjecting the dielectric to etchback until an upper surface of the gate electrode is exposed.

2. (Original) The semiconductor device of Claim 1, wherein

each of the source/drain regions includes a high-concentration impurity diffusion layer and a low-concentration impurity diffusion layer, and

the sidewall is an ion implantation mask for forming the high-concentration impurity diffusion layer.

3. (Original) The semiconductor device of Claim 1, wherein part of the sidewall located on the isolation is at least partly removed so that the sidewall is discontinued.

4. (Original) The semiconductor device of Claim 1, wherein portions of the gate electrode provided on the isolation include a contact formation region that constitutes a portion in contact with a gate contact and a region that is opposed to the contact formation region across the element formation region.

5. (Original) The semiconductor device of Claim 1, wherein the sidewall is provided only on the element formation region and boundary regions of the isolation with the element formation region.

6. (Original) The semiconductor device of Claim 1, wherein between the sidewall and the gate electrode, at least one of an L-shaped sidewall and an offset spacer layer is interposed.

7. (Currently amended) The semiconductor device of Claim 1, wherein the dielectric ~~sidewall~~ is made of a silicon nitride film.

8. (Withdrawn)

9. (Withdrawn)

10. (Withdrawn)

11. (Currently amended) A method for fabricating a semiconductor device provided on a substrate including an element formation region formed of a semiconductor layer and an isolation surrounding the sides of the element formation region, said method comprising the steps of:

(a) forming a gate dielectric on the element formation region;

(b) forming a gate electrode extending from the top of the gate dielectric on the element formation region to above the top of the isolation;

(c) forming a dielectric on the substrate after the step (b);

(d) forming a sidewall surrounding the sides of the gate electrode by subjecting the dielectric to etchback until an upper surface of the gate electrode is exposed; and

~~(d)~~ (e) partly removing part of the sidewall located on a surface region of the substrate excluding the element formation region to discontinue the sidewall~~; and~~

~~(e) implanting ions using the sidewall and the gate electrode as masks after the step (c) or (d), thereby forming first impurity diffusion layers in the element formation region of the semiconductor layer~~.

12. (Currently amended) The method for fabricating a semiconductor device of Claim 19 ~~11~~, said method further comprising, between the step (b) and the step (c), the step of implanting ions using the gate electrode as a mask, thereby forming second impurity diffusion layers in the element formation region,

wherein in the step (f) ~~(e)~~, first impurity diffusion layers including a higher-concentration impurity than the second impurity diffusion layers are formed, and each pair of the first impurity diffusion layer and the second impurity diffusion layer constitutes a source/drain region.

13. (Currently amended) The method for fabricating a semiconductor device of Claim 11, wherein

in the step (b), the gate electrode is formed which includes a contact formation region and a region that is opposed to the contact formation region across the element formation region, both regions being located on the isolation, and

in the step (e) ~~(d)~~, the sidewall is at least partly removed in at least one of the regions of the gate electrode located on the isolation.

14. (Currently amended) The method for fabricating a semiconductor device of Claim 11, wherein in the step (e) ~~(d)~~, the sidewall is removed excluding its portions provided on the

element formation region and boundary regions of the isolation with the element formation region.

15. (Currently amended) The method for fabricating a semiconductor device of Claim 11, said method further comprising, between the step (b) and the step (d) ~~(c)~~, the step of forming at least one of an L-shaped sidewall and an offset spacer layer on the sides of the gate electrode.

16. (Currently amended) The method for fabricating a semiconductor device of Claim 11 wherein the dielectric ~~sidewall~~ is made of a silicon nitride film.

17. (Withdrawn)

18. (Withdrawn)

19. (New) The method for fabricating a semiconductor device of Claim 11, said method further comprising step (f) of implanting ions using the sidewall and the gate electrode as masks after step (d) or (e), thereby forming first impurity diffusion layers in the element formation region of the semiconductor layer.